

Fig. 1
Prior Art

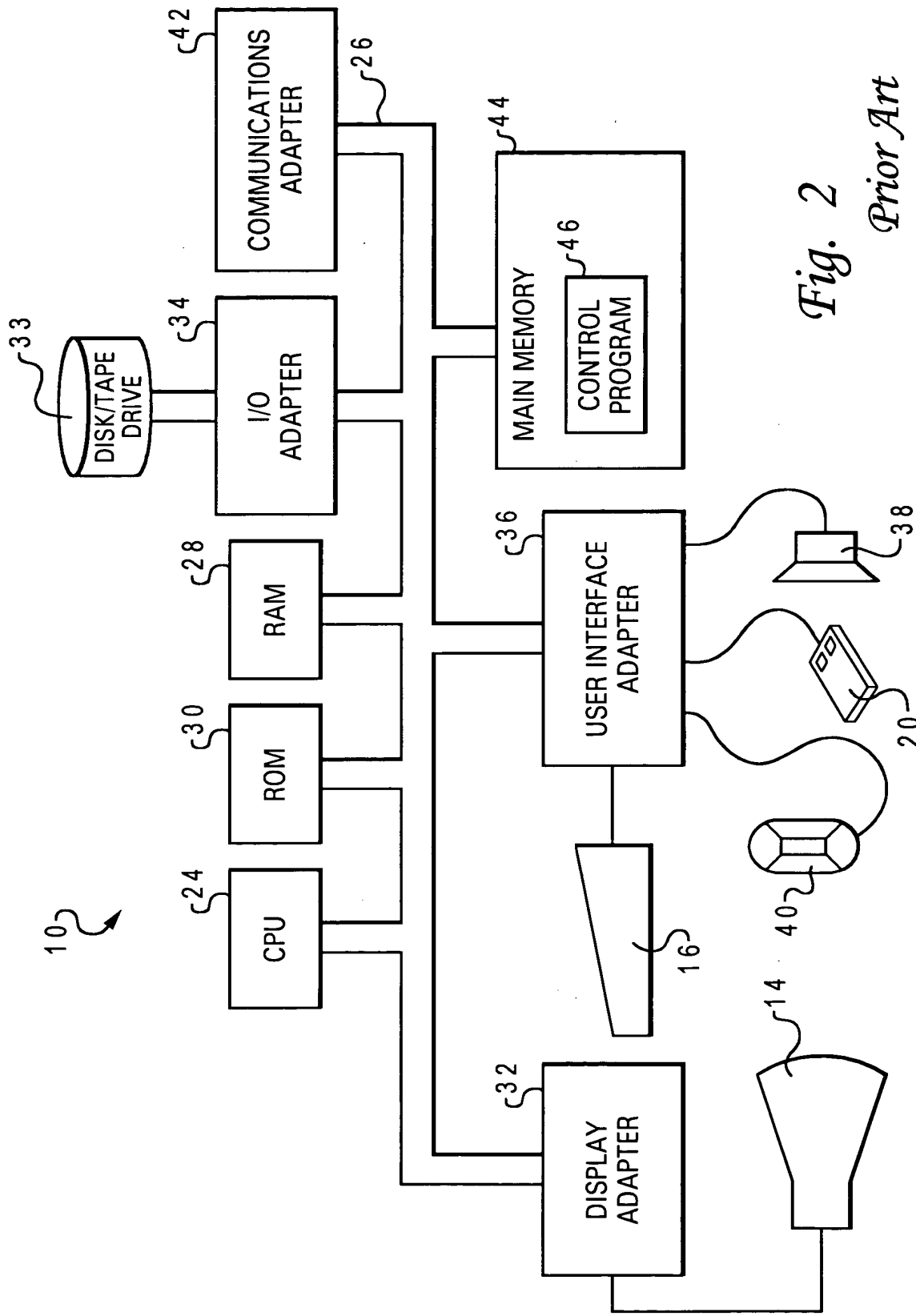


Fig. 2
Prior Art

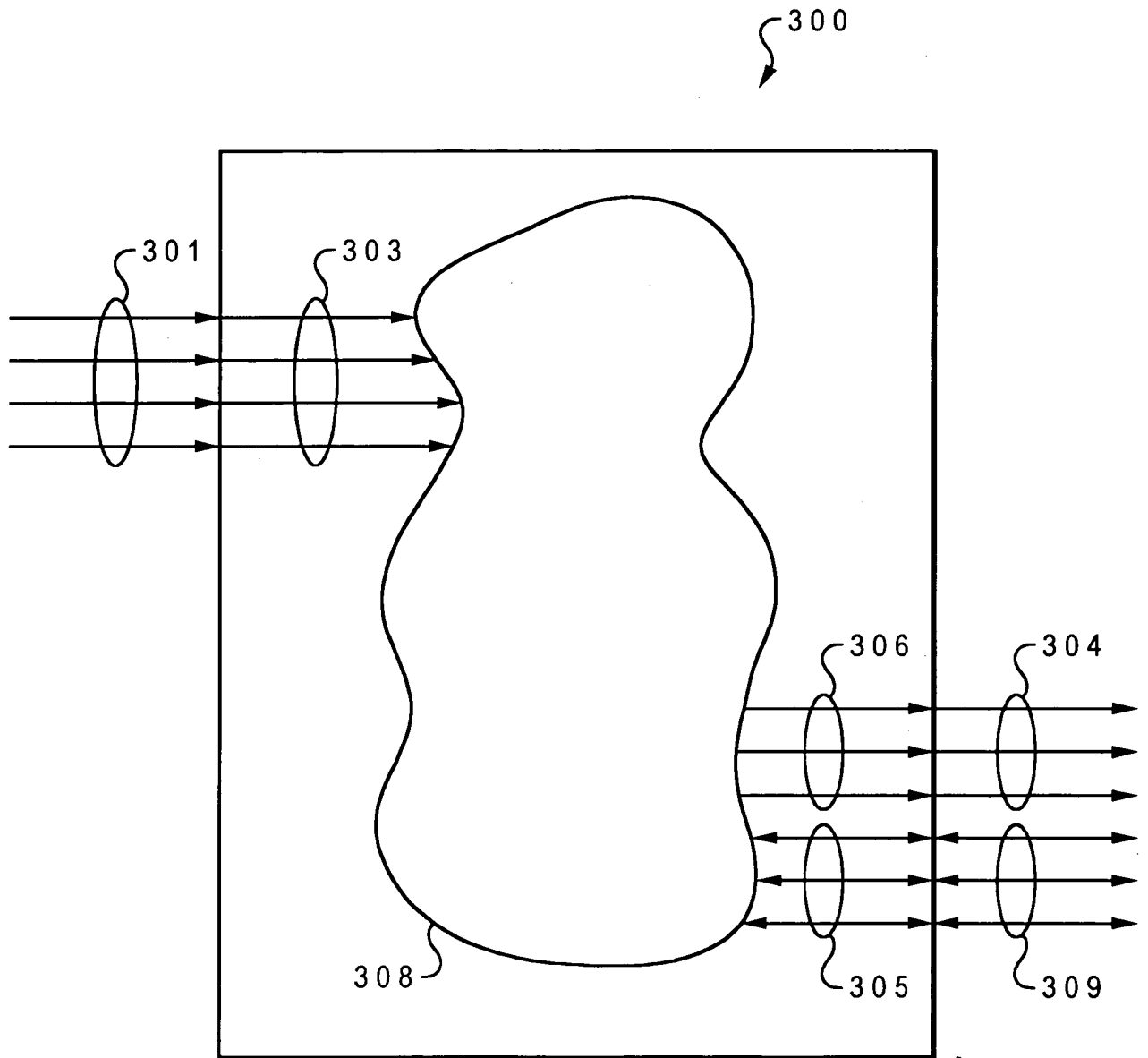


Fig. 3A

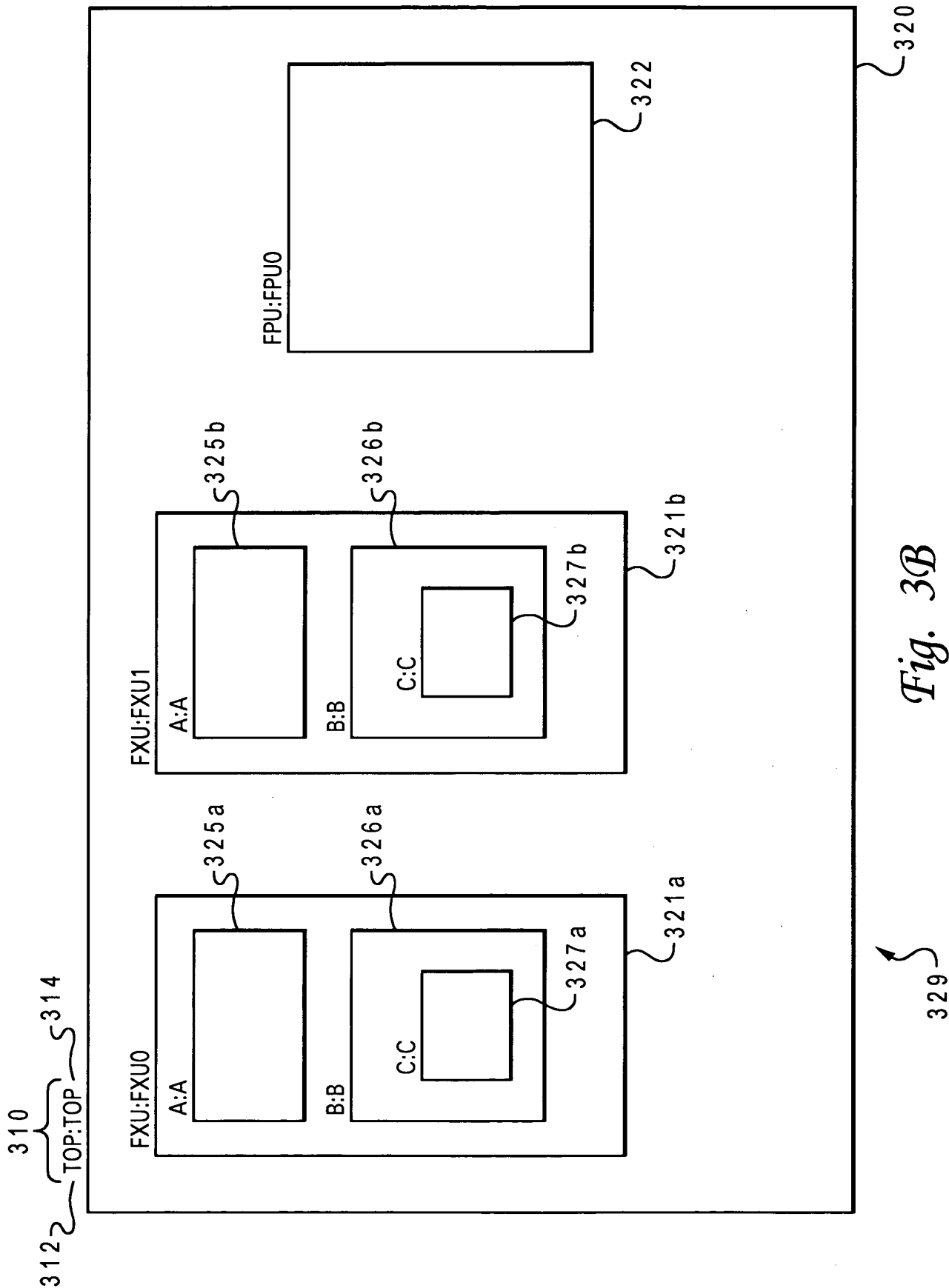


Fig. 3B

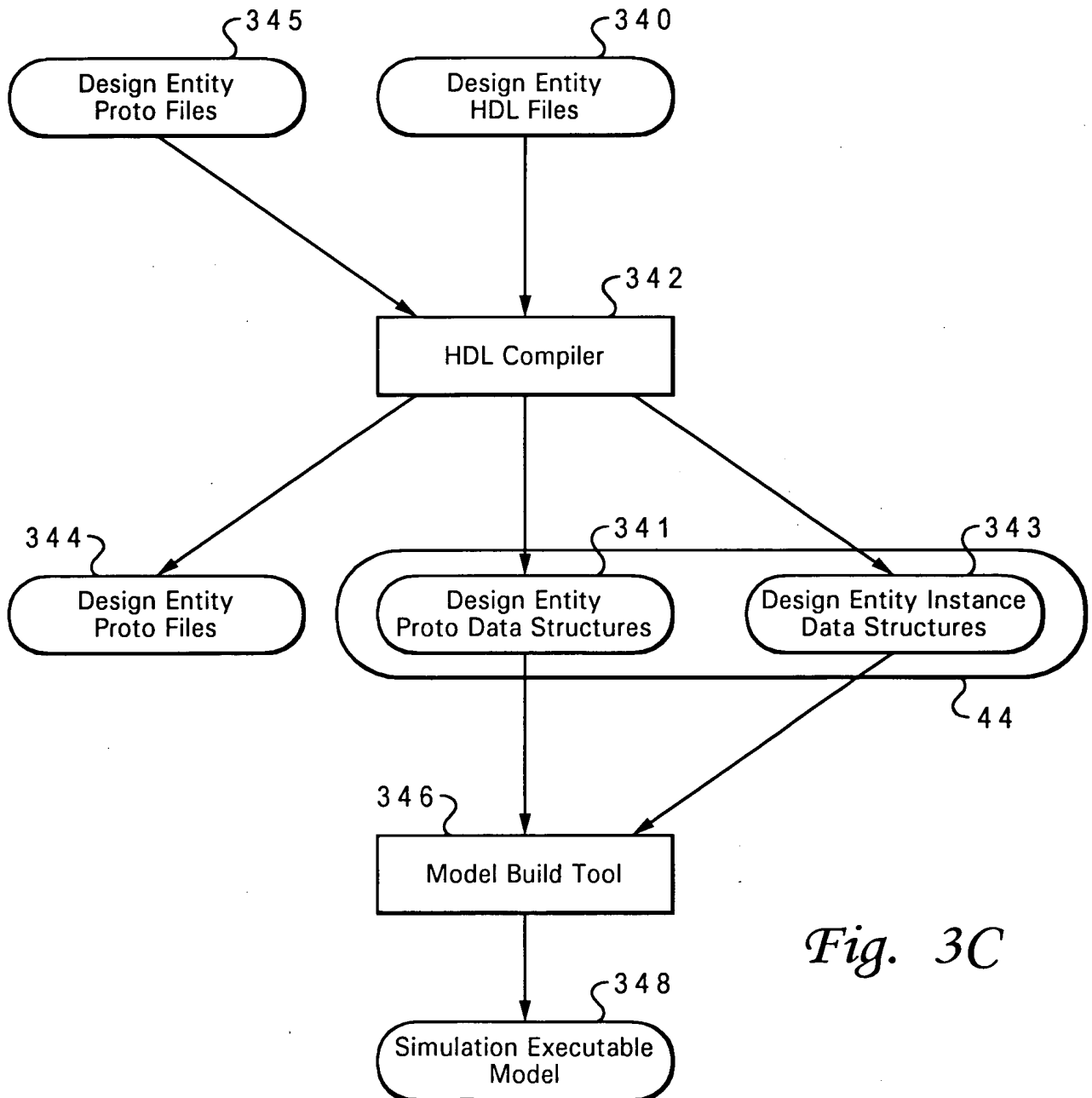


Fig. 3C

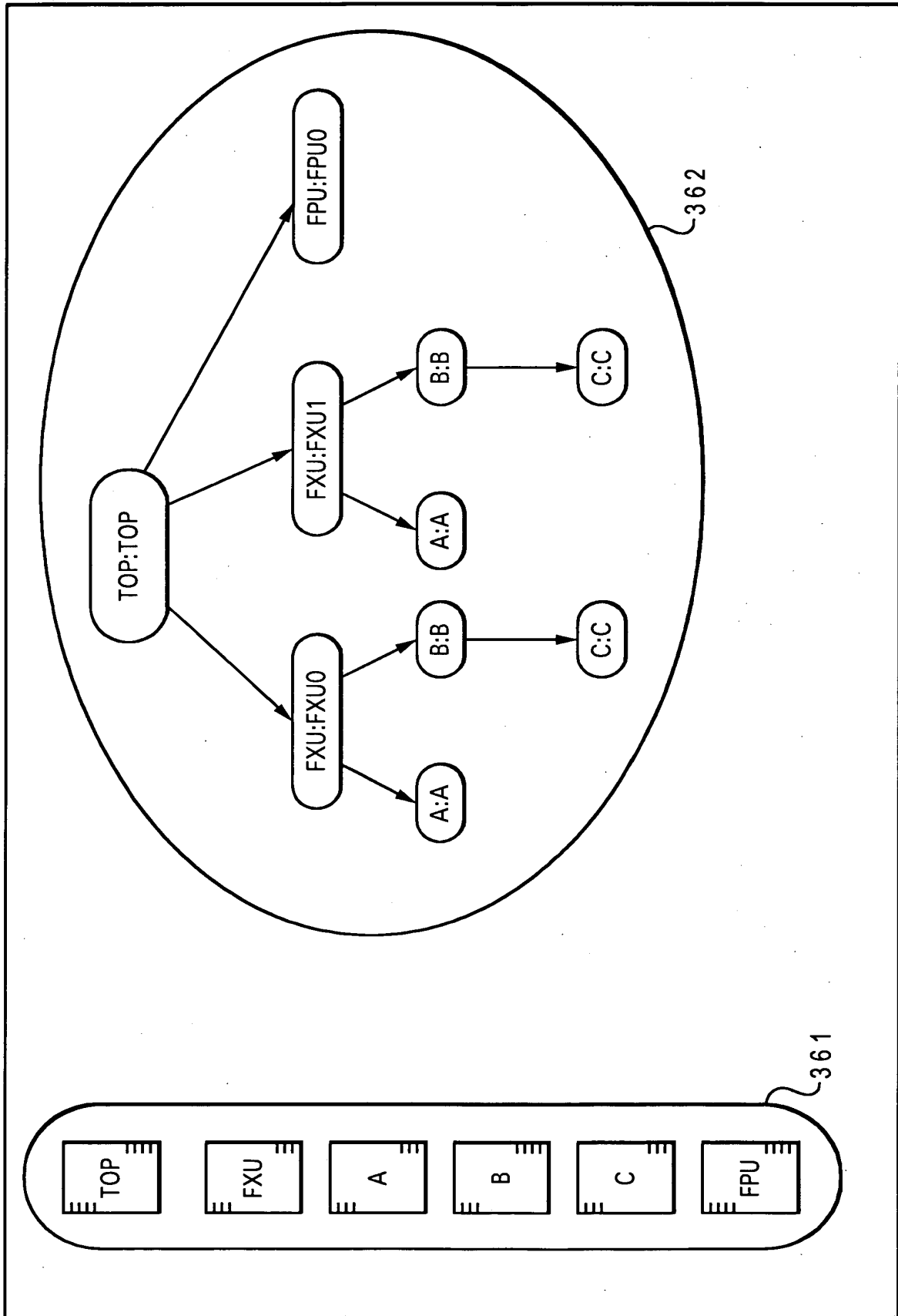


Fig. 3D

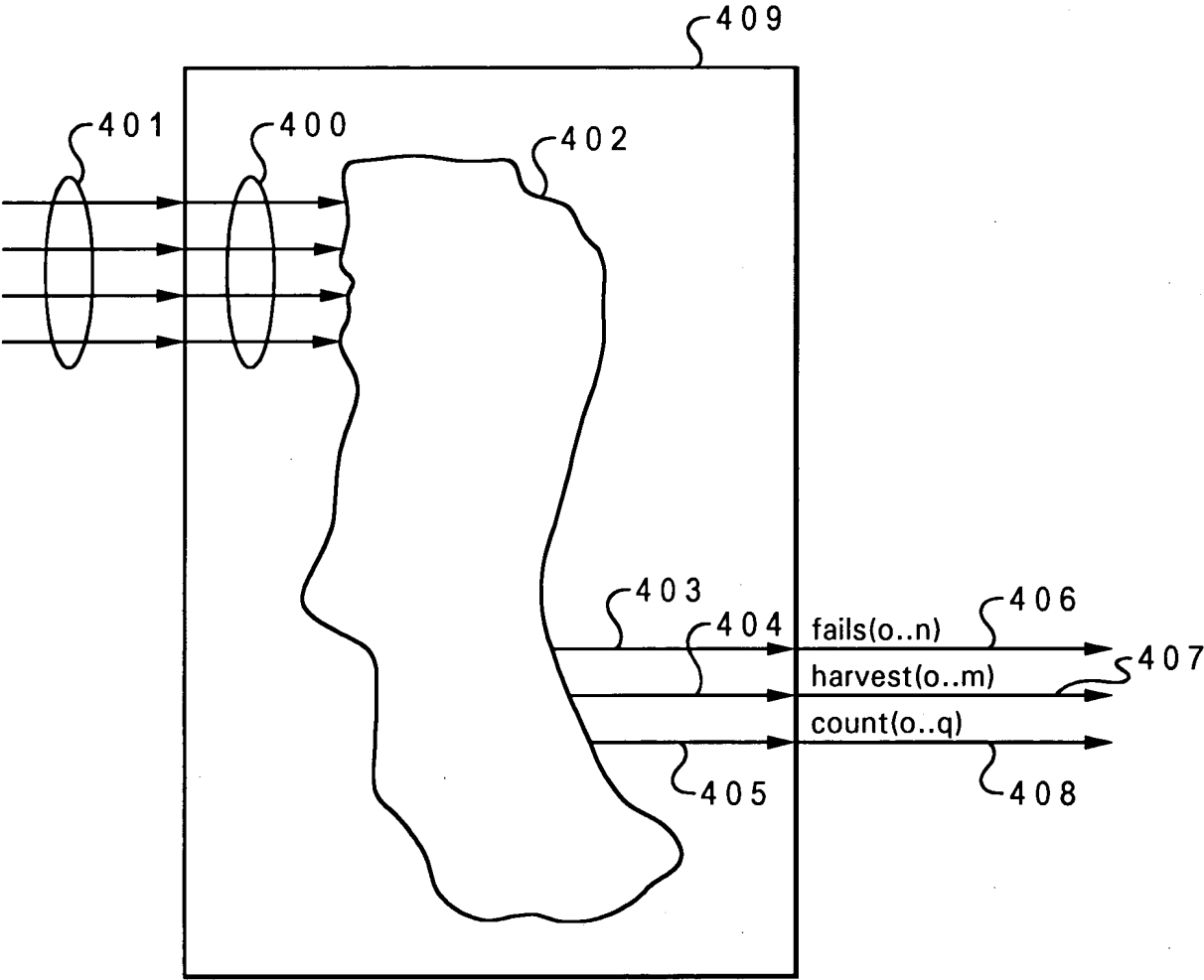
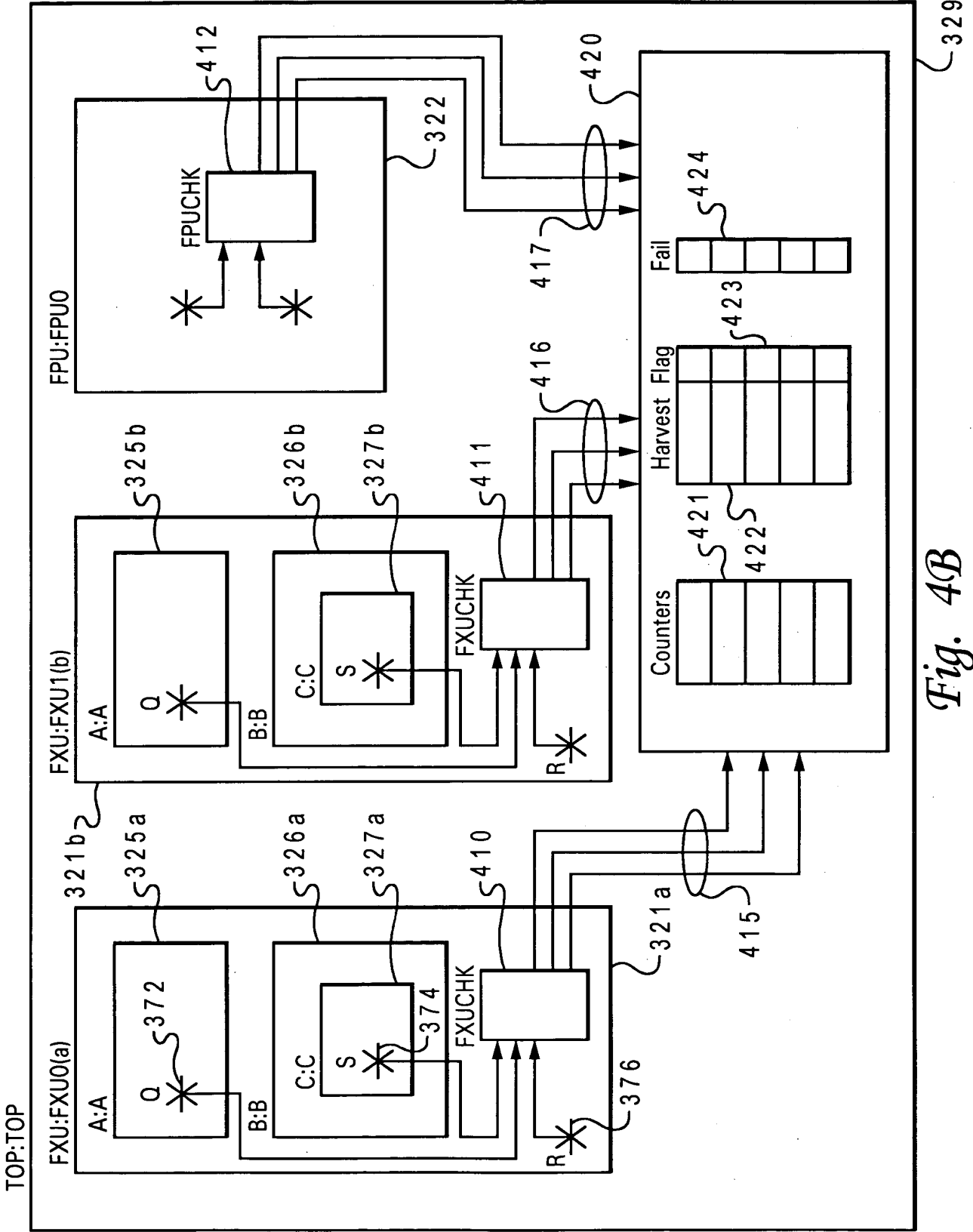


Fig. 4A




```

ENTITY FXUCHK IS
    PORT(
        S_IN      : IN std_ulogic;
        Q_IN      : IN std_ulogic;
        R_IN      : IN std_ulogic;
        clock      : IN std_ulogic;
        fails      : OUT std_ulogic_vector(0 to 1);
        counts     : OUT std_ulogic_vector(0 to 2);
        harvests   : OUT std_ulogic_vector(0 to 1);
    );
4 5 2 { --!! BEGIN
      --!! Design Entity: FXU;

4 5 3 { --!! Inputs
      --!! S_IN      => B.C.S;
      --!! Q_IN      => A.Q;
      --!! R_IN      => R;
      --!! CLOCK     => clock;
      --!! End Inputs

4 5 4 { --!! Fail Outputs;
      --!! 0 : "Fail message for failure event 0";
      --!! 1 : "Fail message for failure event 1";
      --!! End Fail Outputs;

4 5 5 { --!! Count Outputs;
      --!! 0 : <event0> clock;
      --!! 1 : <event1> clock;
      --!! 2 : <event2> clock;
      --!! End Count Outputs;

4 5 6 { --!! Harvest Outputs;
      --!! 0 : "Message for harvest event 0";
      --!! 1 : "Message for harvest event 1";
      --!! End Harvest Outputs;

4 5 7 { --!! End;

ARCHITECTURE example of FXUCHK IS
    BEGIN
        ... HDL code for entity body section ...
    END;

```

4 5 0

4 5 1

4 4 0

4 5 8

Fig. 4C

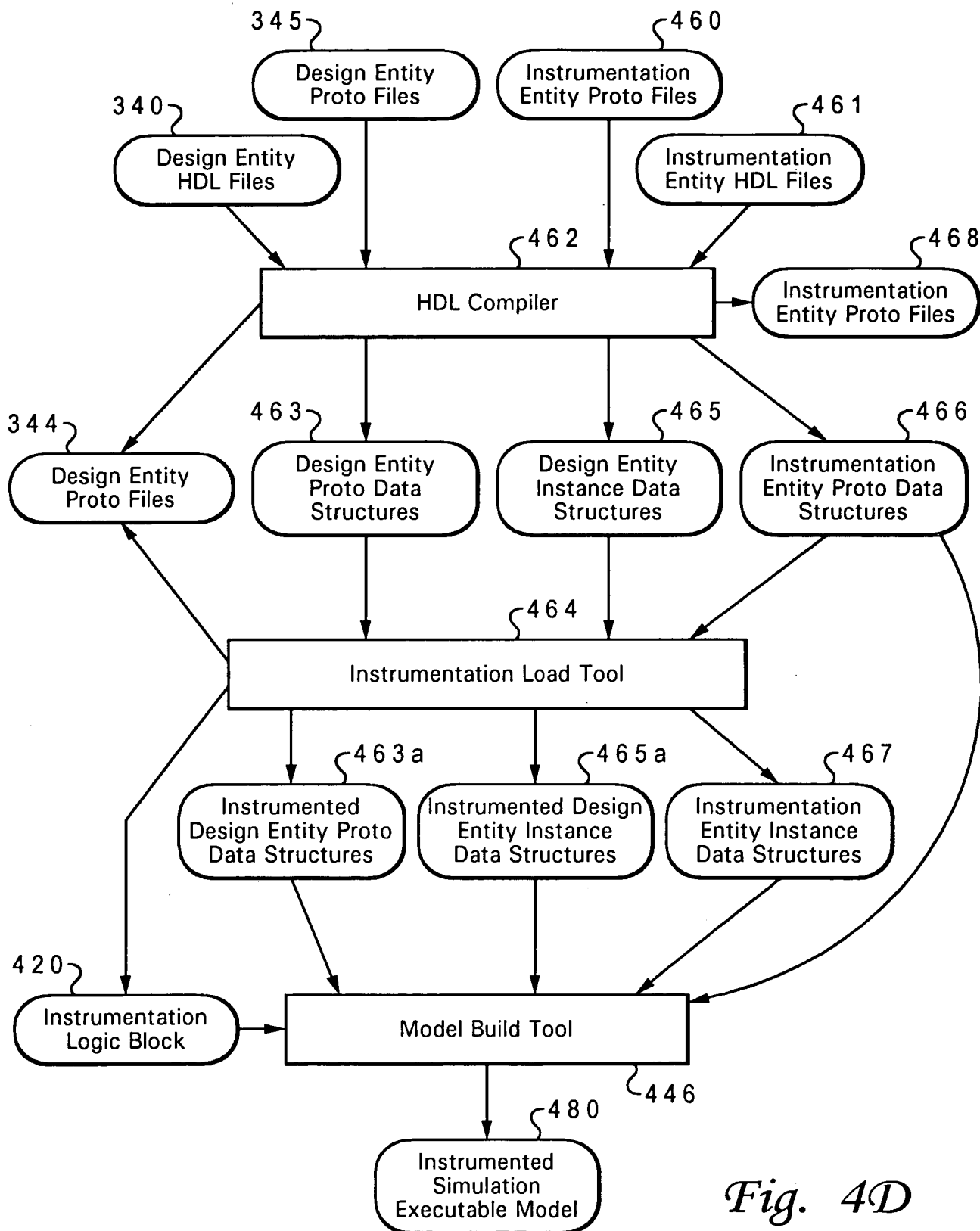
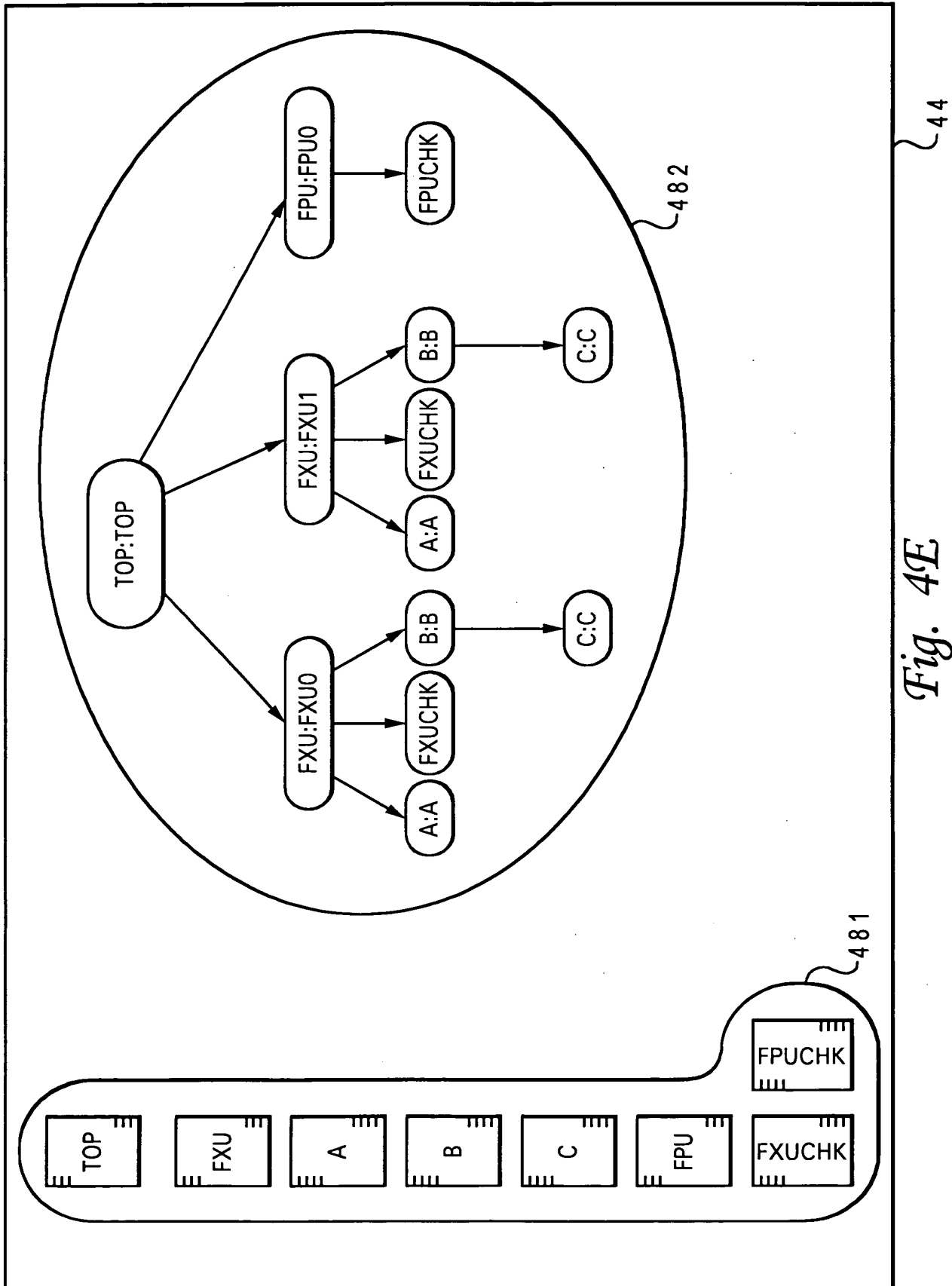


Fig. 4D



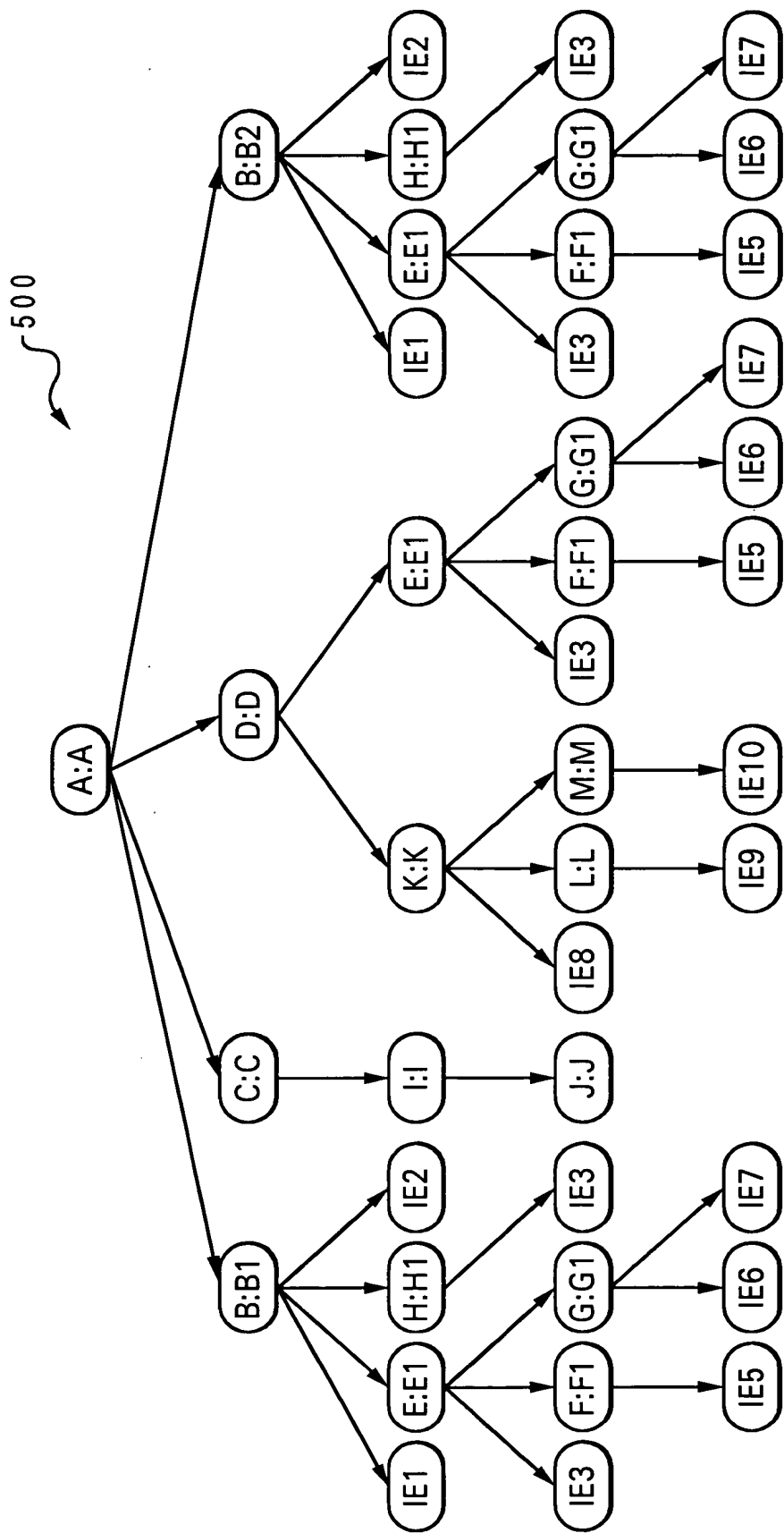


Fig. 5

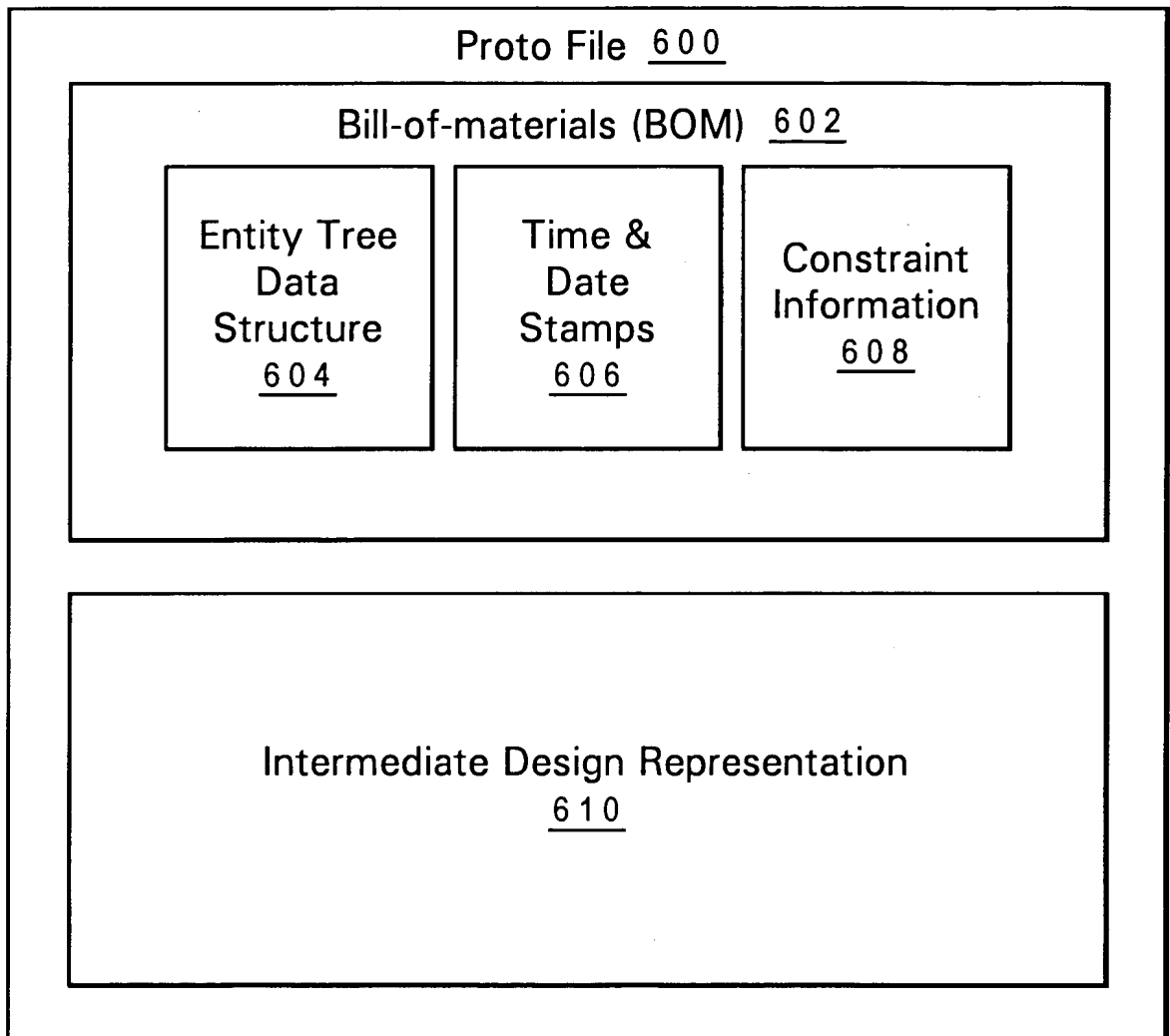


Fig. 6A

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ENTITY	DESCENDANTS
A	B, C, D
B	E, H, {IE1}, {IE2}
C	I
D	K, E
E	F, G, {IE3}
F	{IE5}
G	{IE6}, {IE7}
H	{IE4}
I	J
J	
K	L, M, {IE8}
L	{IE9}
M	{IE10}

Fig. 6B

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ENTITY	SELECTED IEs
A	
B	
C	
D	
E	{IE3}
F	{IE5}
G	{IE6}, {IE7}
H	
I	
J	
K	
L	
M	

Fig. 6D

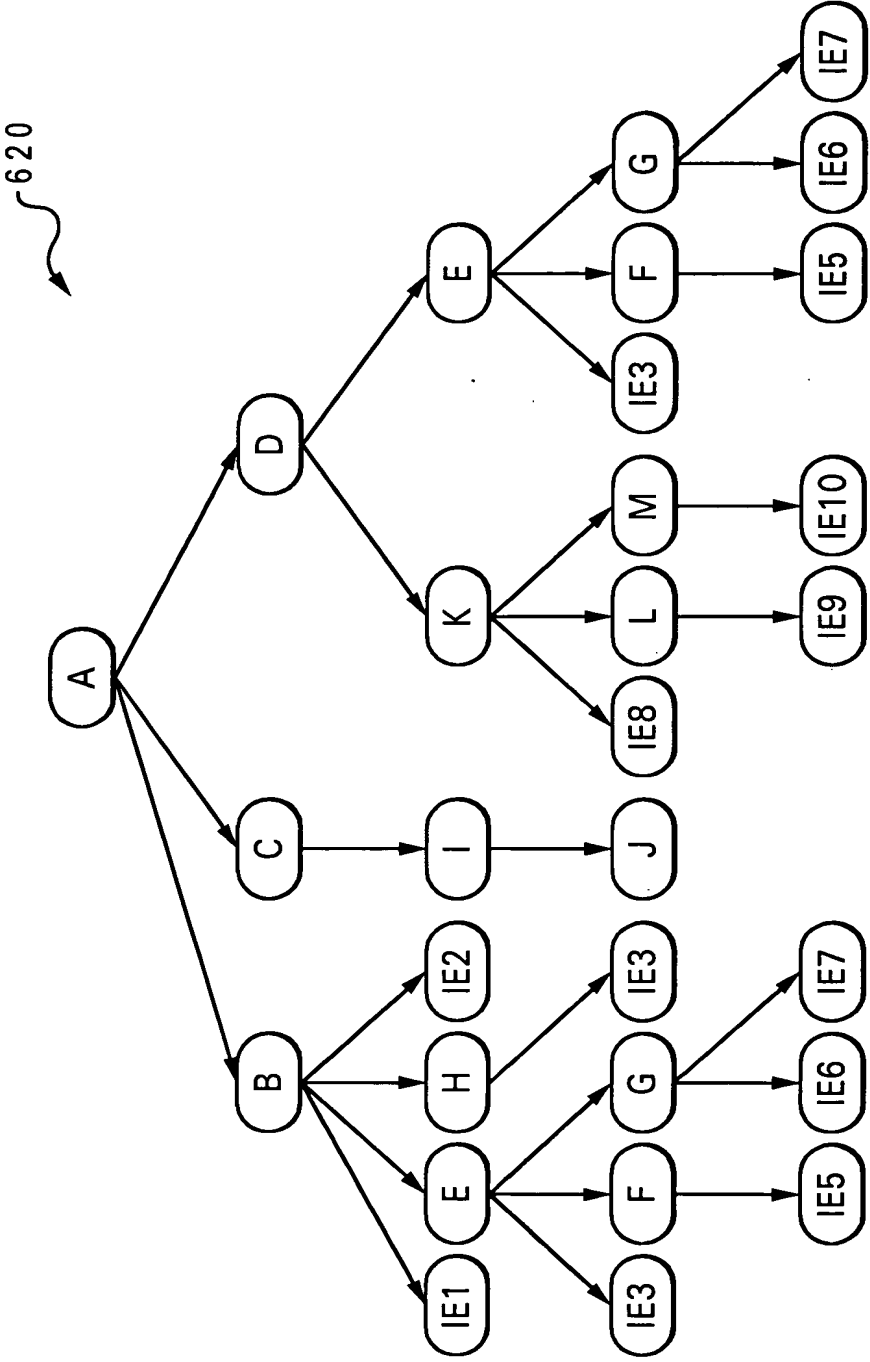


Fig. 6C

Fig. 7

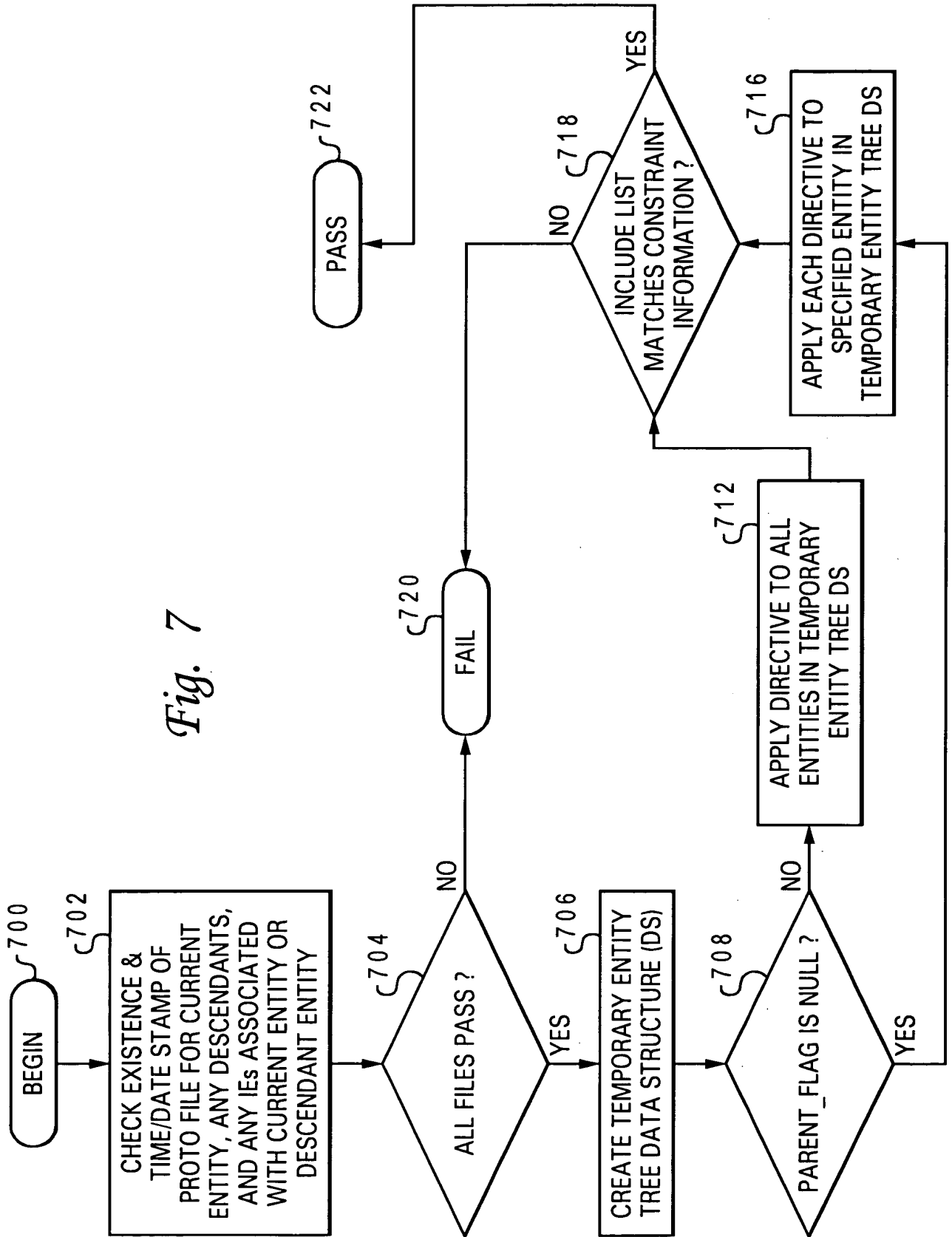


Fig. 8

